A COMPARATIVE STUDY OF CCSA AND OCCSA

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ABSTRACT:
Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. Their performance strongly affects both memory access time, and overall memory power dissipation. As with other ICs today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. This increased bit-line capacitance in turn slows down voltage sensing and makes bit-line voltage swings energy expensive resulting in slower more energy hungry memories. In this paper we are comparing the clamped bit-line sense amplifier and the offset compensated current sense amplifier and studying the advantages and disadvantages of both the current sense amplifiers.

KEYWORDS: Sense amplifier, SRAM, performance.

I.INTRODUCTION

A Sense Amplifier is one of the elements which make up the circuitry on a semiconductor memory chip. It is part of the read circuitry which is used when data is read from the chip. The job of a sense amplifier is to sense the logic levels from a bit-line which represents a data bit (1 or 0) stored in a memory cell on the chip, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly at the output terminal of the chip. Sense amplifier circuits consist of 2 to 6, usually 4 transistors. There is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a chip. It is one of the only analog circuits on a digital memory chip.

The data in a semiconductor memory chip is stored in tiny circuits called memory cells. Sense Amplifiers are primarily applied in Volatile memory cells. The memory cells are either SRAM or DRAM cells which are laid out in rows and columns on the chip. Each line is attached to each cell in the row. The lines which run along the rows are called word-lines which are activated by putting a voltage on it. The lines which run along the columns are called bit-line and two such Complementary bit-lines are attached to a sense amplifier at the edge of the array. Number of sense amplifiers are of that of the bit-line on the chip. Each cell lies at the intersection of a particular word-line and bit-line, which can be used to address it. The data in the cells is read or written by the same bit-lines which run along the top of the rows and columns.

SRAM OPERATION:

To read a bit from a particular memory cell, the word-line along the cell's row is turned on, activating all the cells in the row. The stored value Logic 0 or 1 from the cell then comes to

the Bit-lines associated with it. The sense amplifiers at the end of the two complimentary bit-lines amplify the small voltages to a normal logic level. The bit from the desired cell is then latched from the cell's sense amplifier into a buffer, and put on the output bus.

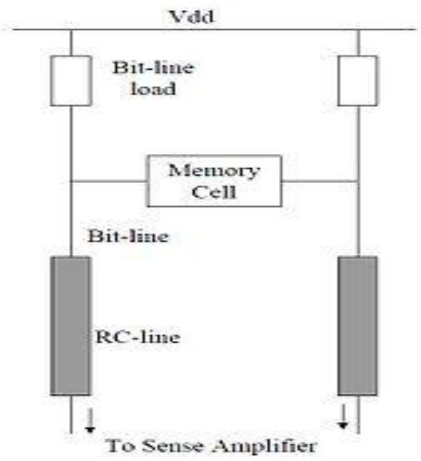

Figure1:Sense Amplifier Position

DRAM OPERATION:

The sense amplifier operation in DRAM is quite similar to the SRAM, but it performs an additional function. The data in DRAM chips is stored as electric charge in tiny capacitors in the memory cells. The read operation depletes the charge in a cell, destroying the data, so after the data is read out the sense amplifier must immediately write it back in the cell by applying a voltage to it, recharging the capacitor. This is called memory refresh.

CURRENT SENSE AMPLIFIER:

Current sense amplifiers are special purpose amplifiers that output a voltage proportional to the current flowing in a power rail. They utilize a current-sense resistor to convert the load current in the power rail to a small voltage, which is then amplified by the current-sense amplifiers. The currents in the power rail can be in the range of 1 A to 20 A, as a result, the current-sense resistor is a very low ohmic value resistor (usually in the range of a 1 mO to 100 mO). These amplifiers are designed to amplify a very small sense voltage in the order of 10 mV to 100 mV in the presence of very large common-mode voltages in the order of 5 V to 30 V. DC precision and high common-mode rejection ratio (CMRR) are distinguishing characteristics of these amplifiers. Current sense amplifiers can either measure current flowing in a single direction or bidirectional amplifiers can measure current flow in both directions through the sense resistor. Traditional differential amplifiers powered between two power supply rails can only process or amplify signals that lie between these two power rails. If any voltage greater than these power supply rails are applied to their input pins, internal ESD protection diodes turn-on, causing large currents to flow and damage these parts.

Due to their great importance in memory performance sense amplifiers have became a very large class of circuits. Their main function is to sense or detect stored data from a read-selected memory cell. The need for increased memory capacity, higher speed, and lower power consumption has defined a new operating environment for future sense amplifiers. Some of the effects of increased memory capacity and decreased supply voltage are 1.Increase in the number of memory cells per bit-line increases CBL, while an increase in length of the bit-line increases RBL 2. Decreasing memory-cell area to integrate more memory on a single chip reduces the current IDATA that is driving the now heavily loaded bit-line. This coupled with increased CBL causes an even smaller voltage swing on the bit-line.3.Decreased supply voltage results in smaller noise margins which in turn affect sense amplifier reliability.

The use of current sensing amplifiers has a number of benefits over voltage sensing amplifiers. The most important ones are

significant reductions in bit-line voltage swing and major reductions in sensing delays [1].These benefits translate to lower dynamic power consumption and increased sensing speed. The key to these improvements lies in the low input resistance of the current sensing amplifier.

II.CLAMPED BIT-LINE CURRENT SENSE AMPLIFIER

The circuit is able to respond very rapidly, as the output nodes of the sense amplifier are no longer loaded with bit-line capacitance. The input nodes of the sense amplifier are low impedance current sensitive nodes. Because of this the voltage swing of the highly capacitance bit-lines change is very small. The improvement in the driving ability of output nodes due to positive feedback and the small difference can be detected and translated to full logic. This is almost insensitive to technology and temperature variations. The main limitation of this circuit is that the bit-lines are pulled down considerably from their pre-charge state through the low impedance NMOS termination. This result in significant amount of energy consumption in charging and discharging the highly capacitive bit-lines. Also, the presence of two NMOS transistors in series with the cross-coupled amplifier results in an increase in the speed of amplification [2].

OPERATION:

The clamped bit-line current sense amplifier is one type of sense amplifier in which we are having two phases. This circuit uses three pre-charge transistors M7, M8, M9 and two current sensing transistors M5 and M6 and four back to back inverter configuration transistors for the voltage output stage. They are reset phase and sense phase. Coming to the operation of the clamped bit-line current sense amplifier in the reset phase the Y sel is kept high and the bit-lines are disconnected from the sense amplifier inputs. The sense amplifier is reset to its meta-stable point by M7, M8, M9 transistors. Between the reset phase and sense phase, in the reset phase the Y sel is driven low while the reset is still kept high. The transistors M8 and M9 keep the sense amplifier at its Meta stable point, while the input current starts to discharge both the bit-lines. A current starts to flow through M7 and slowly ramps up.it can be shown

$$I_{M7}=I_{in}/2[1-\exp(-t/R_{M7}2C_{BL})]$$

Where RM7 is a small signal resistance of M7 in linear region and Iin is the input current at BLb. After IM7 grows large than offset current, reset is pulled to low and sense phase will begin. A conducting path through M7 is shutdown, but the currents through M3, M4, M5, M6 transistors cannot change instantaneously, creating current imbalance between the two branches M1,3 andM2,4.This imbalance of current triggers the regeneration loop formed by M1-M4.

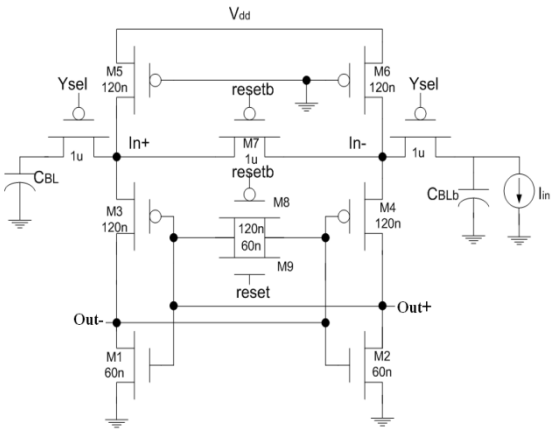

Figure2: clamped bit-line current sense amplifier

The sense time of current sense amplifier is smaller comparing to voltage sense amplifier because large bit-line capacitances are connected to the source nodes of M3,4 and therefore does not load regeneration device. The bit-line

voltages are clamped to the value close to VDD at the end of sense cycle, which saves energy by avoiding to completely discharging bit-lines. However the sense amplifier is not cut-off from supply in reset phase so the current sense amplifier consumes stand-by-power. It also presents a large offset. The transistors M5 and M6 have a negligible effect on offset current compared to M1-M4, because they are in linear region, so their Ids weakly depends on threshold variations. But M1-M4 gives rise to an input offset current. To ensure robustness the input source has to be able to provide current much larger than the offset current variance. The amplifier is bit-line capacitance insensitive maintaining a constant speed over increased bit-line capacitance. The current sense amplifier has a very negligible voltage swing, thus nearly eliminating dynamic power dissipation. The bit-line voltage inactivity significantly decreases cross talk between bit-lines and supply voltage drop associated with bit line charge up [1].The advantages of clamped bit-line current sense amplifier are Access time is less, Less density, Less power consumption, Small sense time, Bit line clamped to a high voltage after sense phase.

The disadvantages of the clamped bit-line current sense amplifier are Reset power, Large offset ,need time margin, This will not work if Iin<Ioffset

III.OFFSET-COMPENSATED CURRENT SENSE AMPLIFIER

Low power SRAMs have become a critical component of many VLSI chips. This is especially true for embedded memories like on-chip caches. The key to low power operation in the SRAM is to reduce the signal swings on the high capacitance bit-lines [3] [4]. This minimum required signal swing is limited by the offset in the sense amplifier. The higher the offset, the higher is the power consumption and the sense delay. This brings us to the typical trade-off between memory yield and power-delay product [5].The offset in sense amplifier is due to transistor mismatch in the supposedly identical matched transistor pair. This mismatch results from process variations such as random dopant number fluctuations, interface-state density fluctuations etc. [6]-[9].

OPERATION:

The offset compensated current sense amplifier is one type of sense amplifier in which we are having two phases. This circuit uses a pre-charge transistor M7 and two current sensing transistors M5 and M6 and four back to back inverter configuration transistors for the voltage output stage. They are reset phase and sense phase. Coming to the operation of the offset compensated current sense amplifier in the reset phase the Ysel is kept high and the bit-lines are disconnected from the sense amplifier inputs. The sense amplifier is reset to its meta-stable point by M7 transistor. Between the reset phase and sense phase, in the reset phase the Ysel is driven low while the reset is still kept high. A current starts to flow through M7 and slowly ramps up. Where RM7 is a small signal resistance of M7 in linear region and Iin is the input current at BLb. After IM7 grows large than offset current, reset is pulled to low and sense phase will begin.

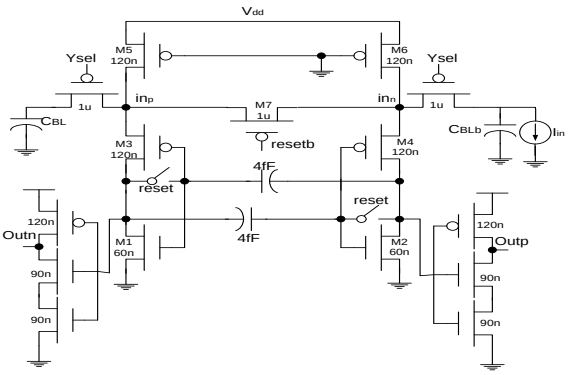

Figure3: offset compensated current sense amplifier

A conducting path through M7 is shutdown, but the currents through M3, M4, M5, M6 transistors cannot change instantaneously, creating current imbalance between the two branches M1,3 and M2,4. This imbalance of current triggers the regeneration loop formed by M1-M4. The sense time of current sense amplifier is smaller comparing to voltage sense amplifier because large bit-line capacitances are connected to the source nodes of M3,4 and therefore does not load regeneration device. The bit-line voltages are clamped to the value close to VDD at the end of sense cycle, which saves energy by avoiding to completely discharging bit-lines. However the sense amplifier is not cut-off from supply in reset phase so the current sense amplifier consumes stand-by-power. It also presents a large offset. The transistors M5 and M6 have a negligible effect on offset current compared to M1-M4, because they are in linear region, so their Ids weakly depends on threshold variations. But M1-M4 gives rise to an input offset current. To ensure robustness the input source has to be able to provide current much larger than the offset current variance. The amplifier is bit-line capacitance insensitive maintaining a constant speed over increased bit-line capacitance. The current sense amplifier has a very negligible voltage swing, thus nearly eliminating dynamic power dissipation. The bit-line voltage inactivity significantly decreases cross talk between bit-lines and supply voltage drop associated with bit line charge up. It has all the benefits of current sense amplifier. But offset contributed by M1-M4 are sampled on the two 4fF offset nulling capacitors in reset phase. In sense phase these two capacitors are in series of the regeneration loop, which effectively removes offset. As a result both input diving capability and the time margin can be significantly reduced from current sense amplifier with reasonable increase in total area.

The advantages of the offset compensated current sense amplifier are No offset, Input current driving capability will be reduced, Time margin will be reduced, Access time is less, Less density, Less power consumption

IV.CONCLUSION

In this paper we have compared the clamped bit-line current sense amplifier and offset compensated current sense amplifier and also explained the operation of both the current sense amplifiers .The clamped bit-line current sense amplifier have some disadvantages like1.consumption of standby power 2.offset current we can overcome these disadvantages by using offset compensated current sense amplifier.

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