

VERILOG BASED DESIGN AND SIMULATION OF PHYSICAL LAYER OF ZIGBEE TRANSRECEIVER

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Abstract: The past several years have witnessed a rapid development in the wireless network area. So far wireless networking has focused on high speed and long range applications. Zigbee technology was developed for Wireless Personal Area Networks (WPAN), aimed at control and military applications with low data rate and low power consumption. Zigbee is standard defines the set of communication protocols for low-data rate short-range wireless networking. Zigbee-based wireless devices operate on 868 MHz, 915 MHz, and 2.4 GHz frequency bands, maximum data rate is 250K bits per second. Zigbee is mainly used for battery-powered applications where low cost, low data rate, and long battery life are main requirements. This paper describes Verilog design for various blocks in Zigbee Transceiver architecture for an acknowledgement frame. The word digital has made a great impact on our society. Developments of digital solutions have possible due to good digital system design and modeling techniques. Further developments have made and introduced VLSI in order to reduce size of the architecture, to improve predictability of the circuit behavior, improvements in speed of operation. Digital Zigbee Transceiver comprises of Cyclic, Bit-to- Symbol block, Redundancy Check, Symbol-to-chip block, Modulator , Pulse shaping block at Transmitter & Demodulation ,Chip synchronization, De-spreading blocks at Receiver. The work here is to show how we can design Zigbee transceiver with its specifications by using Verilog with less number of slices and Look up tables (LUTs).

Keywords: Chip synchronization , De-spreading , LUT , Slices.

1. INTRODUCTION

The past many years have witnessed a fast development within the wireless space network. Wireless networking has been centered on high speed and long vary applications. Zigbee may be a customary that defines the set of communication protocols for low-datarate short-range wireless networking. This is often the most motivation of development of Zigbee customary. The quality Zigbee is developed by the Zigbee Alliance [1]. The Zigbee customary has adopted IEEE 802.15.4 Physical Layer (PHY) and Medium Access Control (MAC) protocols.[3]. The PHY layer supports 3 frequency bands: a.868 MHz band with 1 channel, a 915 MHz band with 10 channels and a 2.45 GHz band with 16 channels.

The word digital encompasses a special place in society. There are two reasons which causes development of digital solution, first is good digital system design and another is modeling techniques. More additional developments have created and introduced VLSI so as to enhance speed of operation, to scale back size of the design, enhancements in sure thing of the circuit behavior. Digital Zigbee Transceiver contains of Cyclic, Bit-to-image block, Redundancy Check, Symbol-to-chip block, Modulator, Pulse shaping block at Transmitter & reception, Chip synchronization, De-spreading blocks at Receiver. The work here is to indicate however we will

style Zigbee transceiver with its specifications by using Verilog with less number of slices and Look up tables (LUTs).

In this, the MAC layer defines 2 forms of nodes: Full perform Devices (FFDs) and Reduced perform Devices (RFDs). The Zigbee networking topologies are classified into chiefly 2 types: peer-to-peer and star. Within the peer-to-peer topology, if the devices are close enough to establish a successful communication link, every device will directly communicate with the other device. Within the star topology, each device will communicate solely with the central personal area network (PAN) arranger within the network. The central node or PAN arranger is FFD and different nodes is RFDs or FFDs. [2].

The IEEE 802.15.4 defines four MAC frame structures: MAC command frames, data, beacon and acknowledgment. The MAC command frame carries MAC commands. The data frame carries data to be transmitted. The coordinator use beacon frame to transmit beacons. The beacons are used for synchronizing the clock of all the devices that square measure within the same network. Within the meantime, the acknowledgement frames is used to make sure successful frame reception [3].

2. DETAILS EXPERIMENTAL

2.1. ZIGBEE TRANSRECEIVER

MAC frame structures carries with it MAC command frames, data, beacon, and acknowledgment. The perform of beacons is to synchronize the clock of all the devices at intervals identical network. The beacon frame is employed for transmitting beacons by a coordinator. The data frame is used for transmitting data . The acknowledgement frame is employed to verify successful frame reception [3]. The MAC commands are transmitted employing a MAC command frame. The Zigbee digital transmitter is meant for associate acknowledgment frame that is shown in Figure 1 supported IEEE 802.15.4 standard.

This and doesnot carry any MAC payload & it is that the simplest MAC frame format. This frame is built from MAC footer (MFR) and MAC header (MHR). The direct sequence number (DSN) and frame control field type the MHR. The MFR is consists of 16-bit frame check sequence (FCS). Each MFR and MHR conjointly called PHY service data unit (PSDU) that becomes the PHY payload. The PHY payload is prefixed with the synchronization header (SHR), consists of preamble sequence, start of frame delimiter (SFD), and PHY header (PHR).The PHY protocol data unit (PPDU) is made by combining SHR, PHR and PHY payload. The Preamble sequence field has length four octets. As for PHR, the length is one octet. The SFD conjointly contains one octet. This can be follows by the MHR and therefore the MFR with 3 octets and 2 octets, severally. Hence, the acknowledgment frame length is completely 11 octets.

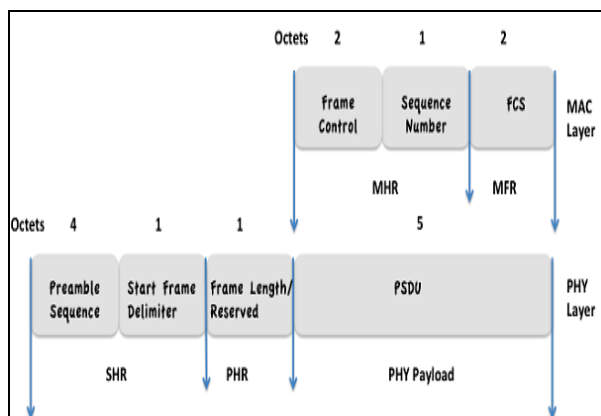


Figure1. The acknowledgment frame [13].

IEEE 802.15.4 standard includes direct sequence spread spectrum (DSSS) [9]. During this paper the acknowledgment frame contains 11 octets (88 bits) of physical protocol data unit (PPDU). The cyclic redundancy check (CRC) block takes binary data as input from PPDU packet to notice errors throughout transmission. CRC is that the most well-liked

methodology of encryption as a result of it provides terribly economical protection against usually occurring burst errors [2], and is well enforced [3]. All one bits and two bits errors in addition as all odd range of bits in error may be detected by CRC's [4]. Since CRC is merely error detection technique not miscalculation correcting technique. Once errors are detected, the total packet data are going to be retransmitted if error happens [6]. For Zigbee standard, CRC includes a division of the transmitted packet data by a continuing known as the generator polynomial [7]. During this paper, the CRC block contains the PHY, SHR and PHR payload. Within the PHY payload, the FCS mechanism uses a 16-bit CRC to notice errors [3]. The FCS is calculated over the MHR and MFR payload components of the frame exploitation the algorithmic program.

2.2. TRANSCEIVER ARCHITECTURE

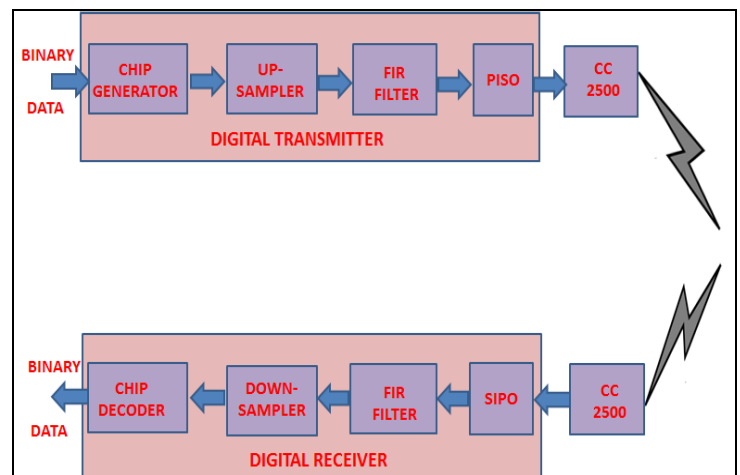


Fig2. Block diagram of zigbee transceiver.

For 2.4 GHz band zigbee applications, sixteen channels are accessible with 5 MHz sample channel spacing .The Transceiver design is shown in fig.2. The binary data is first applied to chip generation block that first maps every four bits into one symbol. Then every symbol is mapped into eight bit p-n chip sequence. Afterward every little bit of p-n sequence is up sampled to match nyquist criteria. The even bits are up sampled by “up sampler- I”, and odd bits are up sampled by “up sampler- Q”.

These up sampled bits area unit suffered separate Fir filters. The output of up sampler-I is suffered filter Fir-I and output of up sampler-Q is suffered filter Fir-Q. These filters area unit nothing however [*fr1] trigonometric function pulse shaping filter’s that is reduces the digital noise. The output of FIR is 10bit block that is then transmitted to “CC2500” module serially by parallel in

serial out (PISO) block. “CC2500” module transmits incoming packets to wireless channel.

At receiver facet “CC2500” receiver module receives the packets serially & serial in parallel out (SIPO) converts the serial packets into parallel blocks. These parallel packets area unit the applied to FIR filter. The output of FIR filter is then down sampled by down sampler. The output of down sampler is that the applied to chip decoder. The chip decoder decodes incoming chip signal and at output provides corresponding four bit symbol. This data is then applied to parallel to serial device which provides serial stream of original binary data sent by transmitter.

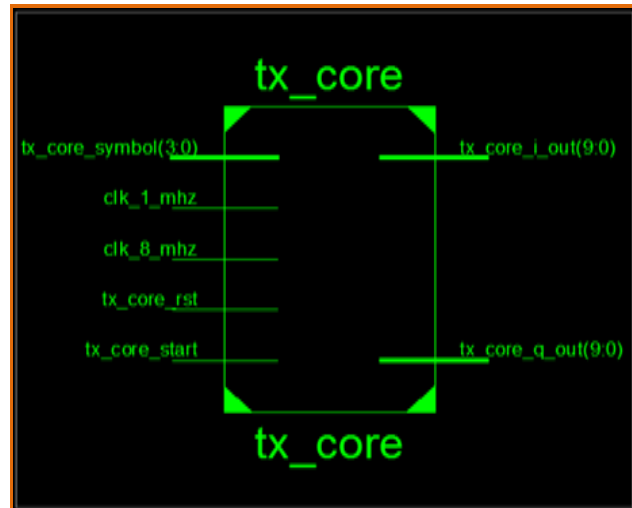


Fig.4. RTL schematic of Zigbee Transmitter

The digital transmitter structure is shown in Fig.4. The “clk_1_mhz” and “clk_8_mhz” are the clock frequencies of 1 MHz and 8 MHz, severally. The input ports are comprised of “tx_core_symbol(3:0)”, “tx_core_rst”, “tx_core_start”. The “tx_core_i_out (9:0)” and “tx_core_q_out (9:0)” are the output ports of I-phase and Q-phase signal, severally.

3.3. Design Utilization Summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	272	1920	14%
Number of Slice Flip Flops	102	3840	2%
Number of 4 input LUTs	509	3840	13%
Number of bonded IOBs	28	141	19%
Number of GCLKs	2	8	25%

Fig.5. Design Utilization Summary of Zigbee Transmitter

CONCLUSIONS

The Transmitter Block of Zigbee Transceiver is developed on Xilinx 13.1 ISE and tested with success. The implementation of transmitter is completed on Xilinx Spartan 3E XC 3S200 FPGA. The information transmission is additionally verified by receiving packets at laptop. The simulation has been performed mistreatment modelsim 6.2 C simulator .The wave form

3. RESULTS AND DISCUSSION

3.1. Simulation Waveforms

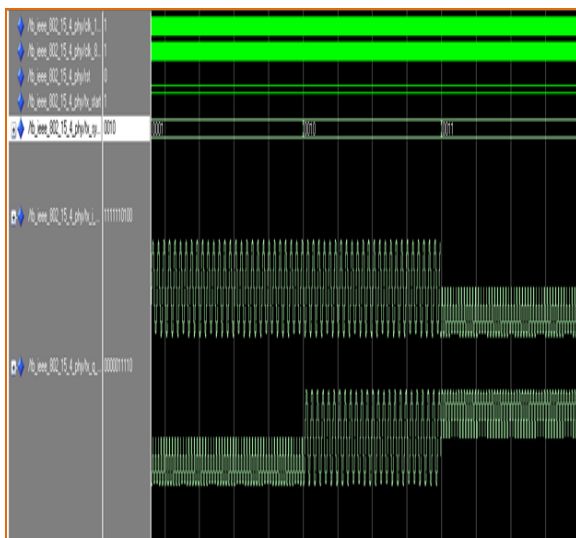


Fig.3. Output Simulation Waveform on Modelsim 6.2C simulator

Fig.3. shows the simulation wave form for zigbee transmitter. The waveforms for I-channel & Q-channel for numerous symbols are shown in figure. For simulation Mentor Graphics “modelsim 6.2 C” tool is employed .The 1 MHz & 8 MHz clocks are applied to transmitter, Logic high is applied to the “start” little bit of transmitter. Then negative edge trigger is applied to “reset” bit.

3.2. RTL Schematic

matches with theoretical expectations. The remaining a part of the transceiver are designed and synthesized in future.

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