ANALYSIS AND SIMULATION OF BUS-CLAMPING PWM TECHNIQUES
BASED ON SPACE VECTOR APPROACH

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Abstract

Conventional space vector pulse width modulation employs conventional switching sequence, which divides the zero vector time equally between the two zero states in every sub cycle. Existing bus-clamping PWM techniques employ clamping sequences, which use only one zero state in a sub cycle. In the present work a new set of BCPWM dealing with a special type of switching sequences, termed as “double-switching clamping sequences”, which use only one zero state and an active vector repeats twice in a sub cycle, will be proposed. It is shown analytically that the proposed BCPWM techniques result in reduced harmonic distortion in the line currents over CSVPWM as well as existing BCPWM techniques at high modulation indices for given a average switching frequency. This work deals with Analysis and Simulation of “double-switching clamping sequences” in terms of stator flux ripple and line current harmonic distortion. Simulation is done on v/f controlled Induction Motor drive in MATLAB/SIMULINK environment.

Index Terms: Bus clamping pulse width modulation (BCPWM), discontinuous PWM, harmonic distortion, induction, motor drives, PWM inverters, space vector PWM, stator flux ripple, switching sequences.

1. INTRODUCTION

Voltage source inverter fed induction motors are widely used in variable speed applications. The harmonic distortion in the motor phase currents must be low for satisfactory operation of the motor drive. The harmonic distortion in the current is determined by the switching frequency and PWM Technique is employed. The switching frequency cannot be increased beyond a certain range due to practical limitations. The distortion is reduced at a given switching frequency by a good design of PWM Technique. This project focuses on developing and evaluating new real time PWM techniques for voltage source inverters.

SPWM and CSVPWM are very popular real time techniques. CSVPWM and THIPWM lead to higher line side voltages for given dc bus voltage compare to SPWM. These technique results in less harmonic distortion in motor currents than SPWM at a given line voltage. Discontinuous modulation methods lead to reduction in distortion at higher line voltages over a CSVPWM for a given average switching frequency. This paper proposes high performance HSVPWM, which further reduce the distortion in the line currents over comparable real-time technique at a given average switching frequency. The superiority in performance of proposed techniques is established theoretically as well as experimentally.

With SPWM, CSVPWM and THIPWM, every phase switches once in a sub-cycle or half carrier signal. This paper explores novel switching sequence that switch ‘a’ phase twice in a sub-cycle, while switching second phase once and clamping the third phase. This paper brings out all such possible sequences (including two new sequences), which results same average switching frequency as CSVPWM for a given sampling frequency.

The proposed hybrid PWM techniques employ the sequence which results in the lowest rms current ripples over given sub cycle, out of given set of sequences. Consequently the total rms current ripple over fundamental cycle is reduced.
2. SWITCHING SEQUENCES OF INVERTER

A three-phase voltage source inverter has eight switching states as shown in Fig. 1. The two zero states (--- and +++), which short the motor terminals, produce a voltage vector of zero magnitude as shown in the figure. The other six states, or the active states, produce an active voltage vector each. These active vectors divide the space vector plane into six sectors and are of equal magnitude as shown. The magnitudes are normalized with respect to the dc bus voltage.

The six active space vectors are represented by the following expression:

$$\vec{V}_k = \frac{2}{3} V_{dc} e^{j(k-1)\frac{\pi}{3}} \quad \text{with} \quad (k=1, \ldots, 6) \quad (1)$$

In space vector-based PWM, the voltage reference, which is sampled once in every subcycle, TS. Given a sampled reference vector of magnitude $V_{REF}$ and angle $\alpha$ in sector I as shown in Fig. 2, the dwell times of active vector 1, active vector 2 and zero vector in the subcycle are given by $T_1$, $T_2$, and $T_z$, respectively, in CSVPWM divides $T_z$ equally between 0 and 7, and employs the switching sequence 0-1-2-7 or 7-2-1-0 in a sub cycle in sector I. The conditions to be satisfied by a valid sequence in sector I are as follows.

1) The active state 1 and the active state 2 must be applied at least once in a sub cycle.

2) Either the zero state 0 or the zero state 7 must be applied at least once in a sub cycle.

3) In case of multiple application of an active state, the total duration for which the active state is applied in a sub cycle must satisfy (1).

4) The total duration for which the zero vector (either using the zero state 0 or the zero state 7) is applied in a sub cycle must satisfy (1).

5) Only one phase must switch for a state transition.

6) The total number of switching’s in a sub cycle must be less than or equal to three. This ensures that the average switching frequency is less than or equal to that of CSVPWM for a given sampling Frequency.

From the Volt-time balance principle $T_1$, $T_2$ and $T_z$ can be given as

$$T_1 = V_{ref} * T_s * \frac{\sin(60^\circ - \alpha)}{\sin(60^\circ)}$$

$$T_2 = V_{ref} * T_s * \frac{\sin(\alpha)}{\sin(60^\circ)}$$

$$T_z = T_s - T_1 - T_2 \quad (2)$$
3. MODERN PWM TECHNIQUES

The modern PWM methods can be separated into two groups and those are:

- Continuous PWM (CPWM) methods
- Discontinuous PWM (DPWM) methods

In discontinuous one the modulation wave of a phase has at least one segment which is clamped to the positive or negative dc bus for at most a total of 120° (over a fundamental cycle). Where as in continuous PWM there is no clamping in the modulation wave.

The expressions for the modulation signals are given as

$$M_{\text{in}} = \frac{2V_{\text{in}}}{V_{\text{dc}}} + (1 - 2\mu) - \frac{2\mu V_{\text{min}}}{V_{\text{dc}}} + \frac{2(\mu - 1)V_{\text{max}}}{V_{\text{dc}}}$$

(4)

The selection of $\mu$ gives rise to an infinite number of PWM modulations. To obtain the generalized discontinuous modulation signal, $\mu$ is given as:

$$\mu = 1 - 0.5 [1 + \text{sgn}(\cos(3(\omega t + \delta)))]$$

(3)

When $\mu = 0$, any one of the phases is clamped to positive dc bus for 120° and then DPWMMAX is obtained. When $\mu = 1$, any one of the phases is clamped to negative dc bus for 120° and then DPWMMIN is obtained. If $\mu = 0.5$, then the SVPWM algorithm is obtained. Similarly, the variation of modulation phase angle $\delta$ yields to infinite number of DPWM methods. If $\delta = 0, -\pi/6, -\pi/3$, then DPWM1, DPWM2 and DPWM3 can be obtained respectively. The modulation waveforms of the different PWM methods are as shown in Fig. 5.

<table>
<thead>
<tr>
<th>Sector</th>
<th>Conventional sequence</th>
<th>Clamping sequences</th>
<th>Double-switching clamping sequences</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>(012, 723)</td>
<td>(012, 210, 721, 127)</td>
<td>(012, 1210, 7112, 2127)</td>
</tr>
<tr>
<td>II</td>
<td>(7221, 7230)</td>
<td>(7225, 7230, 7122, 220)</td>
<td>(7232, 7237, 7212, 320)</td>
</tr>
<tr>
<td>III</td>
<td>(034, 743)</td>
<td>(034, 343, 743, 437)</td>
<td>(0343, 3430, 7434, 4347)</td>
</tr>
<tr>
<td>IV</td>
<td>(7450, 054)</td>
<td>(745, 547, 554, 545)</td>
<td>(7454, 4547, 0545, 5490)</td>
</tr>
<tr>
<td>V</td>
<td>(0567, 7650)</td>
<td>(056, 650, 765, 567)</td>
<td>(0565, 6500, 7656, 5650)</td>
</tr>
<tr>
<td>V1</td>
<td>(7660, 010)</td>
<td>(761, 160, 010, 610)</td>
<td>(7610, 6100, 0101, 1030)</td>
</tr>
</tbody>
</table>
Fig. 5. Modulation waveforms of the various PWM methods

The conventional SVPWM algorithm employs equal division of zero voltage vector times within a sampling period or sub cycle. However, by utilizing the freedom of zero state division, various DPWM methods can be generated. GDPWM algorithm, which uses the utilization of the freedom of zero state time division. In this proposed method the zero state time will be shared between two zero states as $T_0$ for $V_0$ and $T_7$ for $V_7$ respectively, and $T_0, T_7$ can be expressed as:

$$T_0 = \frac{T}{2} \mu$$

$$T_7 = T \left(1 - \mu\right)$$

(5)

4. BUS-CLAMPING PWM TECHNIQUES

A popular existing bus-clamping method clamps every phase during the middle 30° duration in every quarter cycle of its fundamental voltage. This technique, termed as and “30° clamp.” This employs sequences 721, 127, in the first half, and 012, 210, in the second half of sector I as shown in Fig. 6.

In Fig. 7(a), every phase is clamped continually for 60° duration in every half cycle of the fundamental voltage waveform. These techniques can be termed “continual clamping” techniques. In Fig. 7(b), the 60° clamping duration is split into one interval of width in the first quarter cycle and another interval of $(60° - \gamma)$ in the next quarter in every half cycle. Since the clamping duration is split into two intervals, these techniques are termed “split clamping” PWM techniques. Fig. 8(a) and (b) present average pole voltage waveforms that illustrate the two types of clamping for $\gamma = 45°$.

Fig. 6. Existing bus-clamping PWM technique (30° clamp).

Fig. 7. Existing bus-clamping PWM techniques

(a) Continual clamping type  (b) split clamping type.
Fig. 8. Average pole voltage over a fundamental cycle for \( V_{\text{REF}} = 0.75 \) corresponding to (a) continual clamping and (b) split clamping both with \( \gamma = 45^\circ \).

The design of the inverter phase voltage and common mode voltages for different pulse sequences are:

\[
\begin{align*}
V_{an} &= \frac{V_{dc}}{6} (2S_a - S_b - S_c) \\
V_{bn} &= \frac{V_{dc}}{6} (2S_b - S_c - S_a) \\
V_{cn} &= \frac{V_{dc}}{6} (2S_c - S_a - S_b) \\
V_{com} &= \frac{V_{dc}}{6} (S_a + S_b + S_c)
\end{align*}
\]

(6)

\[ E_{ag} = k_f \phi_{ag} \]

\[ \phi_{ag} = \text{constant} \Rightarrow \frac{E_{ag}}{f} \approx \frac{V}{f} \]

Speed is varied by varying the frequency; maintain v/f constant to avoid saturation of flux. With constant v/f ratio, motor develops a constant maximum torque.

**INDUCTION MOTOR MODELLING**

Among the various reference frames, V/F uses the stationary reference frame. Hence, in this work, the induction motor model is developed in the stationary reference frame, which is also known as Stanley reference frame. Rotor and stator voltages and their flux linkages are

\[
\begin{align*}
\nu = R_s \nu + \frac{d\psi}{dt} \\
\psi = L_s \nu + L_m \nu \\
\psi = L_s \nu + L_m \nu \\
\psi = L_s \nu + L_m \nu \\
\psi = L_s \nu + L_m \nu
\end{align*}
\]

The electromagnetic torque of the induction motor is given by

\[
T_e = T_L + J \frac{d\omega_m}{dt} = T_L + \frac{2}{P} \int \frac{d\omega}{dt}
\]

The Electromechanical equation of induction drive is given by

\[
T_e = \frac{3}{2} \left( \frac{P}{2} \right) \left( \psi d_q i_d - \psi q_s i_d \right)
\]

**VOLTS/HZ CONTROL TECHNIQUE:**

This is the most popular method of Speed control because of simplicity. The Flux and Torque are also function of frequency and voltage respectively the magnitude variation of control variables only. The air gap voltage of induction motor is
5. ANALYSIS OF HARMONIC DISTORTION

The generalized stator q-axis and d-axis flux ripples are as shown below.

\[ Q_1 = [\cos(\alpha) - V_{ref}]*T1 \]

\[ Q_2 = [\cos(60^\circ - \alpha) - V_{ref}]*T2 \]

\[ QZ = -V_{ref}*T2 \]

\[ D = \sin(\alpha)*T1. \]

**Expressions for RMS Stator Flux Ripple:**

The rms stator flux ripples different sequences employed and their respective vector diagram of d-axis and q-axis ripples shown in Fig 12.

\[ F^2_{0127} = \frac{1}{3} \left[ (0.5Q_1)^2 \frac{T_s}{2T_s} + \frac{1}{3} \left[ (0.5Q_1)^2 + 0.5Q_1(0.5Q_1 + Q_1) + (0.5Q_1 + Q_1)^2 \right] \frac{T_s}{T_s} \right. \]

\[ + \frac{1}{3} \left[ (0.5Q_1 + Q_1)^2 - (0.5Q_1 + Q_1)(0.5Q_1) + (-0.5Q_1)^2 \right] \frac{T_s}{T_s} \]

\[ + \frac{1}{3} \left[ (0.5Q_1 + Q_1)^2 \frac{T_s}{2T_s} + \frac{1}{3} \left[ D^2(T_1 + T_2) \right] \frac{T_s}{T_s} \right] \]

\[ (7a) \]

\[ F^2_{012} = \frac{1}{3} \left[ Q_1^2 \frac{T_s}{T_s} + \frac{1}{3} \left[ Q_1^2 + Q_1(Q_1 + Q_1) + (Q_1 + Q_1)^2 \right] \frac{T_s}{T_s} \right. \]

\[ + \frac{1}{3} \left[ (Q_1 + Q_1)^2 \frac{T_s}{T_s} + \frac{1}{3} \left[ D^2(T_1 + T_2) \right] \frac{T_s}{T_s} \right] \]

\[ (7b) \]

\[ F^2_{212} = \frac{1}{3} \left[ Q_1^2 \frac{T_s}{T_s} + \frac{1}{3} \left[ Q_1^2 + Q_1(Q_1 + 0.5Q_1) + (Q_1 + 0.5Q_1)^2 \right] \frac{T_s}{T_s} \right. \]

\[ + \frac{1}{3} \left[ (Q_1 + 0.5Q_1)^2 - (Q_1 + 0.5Q_1)(0.5Q_1) + (-0.5Q_1)^2 \right] \frac{T_s}{T_s} \]

\[ + \frac{1}{3} \left[ (0.5Q_1)^2 \frac{T_s}{2T_s} + \frac{1}{3} \left[ (0.5D)^2 \frac{T_s}{T_s} \right] \right] \]

\[ (7c) \]

\[ F^2_{0121} = \frac{1}{3} \left[ (0.5Q_1)^2 \frac{T_s}{2T_s} + \frac{1}{3} \left[ (0.5Q_1)^2 + (Q_1 + 0.5Q_1)(0.5Q_1) + (Q_1 + 0.5Q_1)^2 \right] \frac{T_s}{T_s} \right. \]

\[ + \frac{1}{3} \left[ (Q_1 + 0.5Q_1)^2 - (Q_1 + 0.5Q_1)(0.5Q_1) + (-0.5Q_1)^2 \right] \frac{T_s}{T_s} \]

\[ + \frac{1}{3} \left[ (0.5Q_1)^2 \frac{T_s}{2T_s} + \frac{1}{3} \left[ (0.5D)^2 \frac{T_s}{T_s} \right] \right] \]

\[ (7d) \]
Fig. 12. Stator flux ripple vector over a subcycle for sequences (a) 0127, (b) 012, (c) 721, (d) 0121 and (e) 7212.

A. Analysis of Existing BCPWM Techniques:

Sequence 012 leads to less RMS current ripple over a subcycle than 721 in the first half of the sector, and vice versa in the second half of the sector.

\[
F_{012}(\alpha) < F_{721}(\alpha), \quad 0^0 < \alpha < 30^0 \quad (8a)
\]

\[
F_{012}(\alpha) > F_{721}(\alpha), \quad 30^0 < \alpha < 60^0 \quad (8b)
\]

\[
F_{012}(\alpha) = F_{721}(60^0 - \alpha) \quad (9)
\]
B. Analysis of Proposed BCPWM Techniques:

\[ F_{0121}(\alpha) < F_{7212}(\alpha) , \quad 0^0 < \alpha < 30^0 \]  
(10a)

\[ F_{0121}(\alpha) > F_{7212}(\alpha) , \quad 30^0 < \alpha < 60^0 \]  
(10b)

\[ F_{0121}(\alpha) = F_{7212}(60^0-\alpha) \]  
(11)

Table 3: Measured Values of \( I_{THD} \) for Proposed BCPWM

6. INVERTER SWITCHING LOSSES

This section presents a comparison of inverter switching losses due to CSVPWM, existing BCPWM techniques. The switching energy loss in a subcycle in an inverter leg is proportional to the phase current and the number of switchings of the phase \( n \) in the given subcycle. The normalized switching energy loss per subcycle \( E_{SUB} \) in an inverter leg is defined in (1a), where \( I_1 \) is the fundamental phase current, \( I_m \) is the peak phase fundamental current and \( \Phi \) is the line-side power factor angle.

\[
E_{SUB} = \frac{n|I_1|}{I_m} = n|\sin(o\tau - \Phi)| \quad (12a)
\]

\[
E_{SUB(AV)} = \frac{1}{\Pi} \int_0^{\Pi} E_{SUB} d\omega \tau \quad (12b)
\]

Fig.16. Variation of normalized switching loss \( E_{SUB} \) over a fundamental cycle for CSVPWM.
Average Switching Loss for CSVPWM = 0.6366

Table 4: Measured Values of Average Switching Loss

7. CONCLUSION

A class of bus-clamping PWM (BCPWM) techniques, which employ only the double-switching clamping sequences, is proposed. The proposed BCPWM techniques are studied, and are compared against conventional space vector PWM (CSVPWM) and existing BCPWM techniques at a given average switching frequency. The proposed families of BCPWM techniques result in less line current distortion than CSVPWM and the existing BCPWM techniques at high line voltages close to the highest line side voltage during linear modulation. The analysis presented explains the difference in distortion due to the different techniques. The study classifies both the existing BCPWM and the proposed BCPWM techniques into two categories, namely continual clamping methods and split clamping methods, depending on the type of clamping adopted. It is shown that split clamping methods are better than continual clamping ones in terms of line current distortion. In terms of switching losses, continual clamping is better at high power factors, while split clamping is superior at low power factors.

REFERENCES


BIOGRAPHIES

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